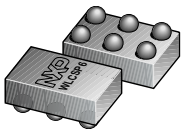


BGS8L4UK

SiGe:C Low Noise Amplifier MMIC with bypass switch for LTE

Rev. 1 — 1 December 2015 Product data sheet

1. Product profile

1.1 General description

The BGS8L4UK is a Low Noise Amplifier (LNA) with bypass switch for LTE receiver applications, available in a Wafer Level Chip-Scale Package (WLCSP). The BGS8L4UK requires one external matching inductor.

The BGS8L4UK delivers system-optimized gain for both primary and diversity applications where sensitivity improvement is required. The high linearity of this low noise device ensures the required receive sensitivity independent of cellular transmit power level in Frequency Division Duplex (FDD) systems. When receive signal strength is sufficient, the BGS8L4UK can be switched off to operate in bypass mode at a 1 μA current, to lower power consumption. The BGS8L4UK requires only one external matching inductor.

The BGS8L4UK is optimized for 720 MHz to 960 MHz.

1.2 Features and benefits

- Operating frequency from 720 MHz to 960 MHz
- Noise figure (NF) = 0.8 dB
- Gain 17.3 dB
- High input 1 dB compression point of –5.0 dBm
- Bypass switch insertion loss of –1.8 dB
- $IP3_i$ of 1.0 dBm
- Supply voltage 1.5 V to 3.1 V
- Integrated supply decoupling capacitor
- Optimized performance at a supply current of 4.4 mA
- Bypass mode current consumption < 1 μA
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and Output AC coupled
- ESD protection on all pins (HBM > 2 kV)
- Integrated matching for the output
- Extremely small Wafer Level Chip-Scale Package (WLCSP)
  6 bumps; 0.69 mm × 0.44 mm × 0.29 mm; 0.25 mm / 0.26 mm bump pitch
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level of 1

1.3 Applications

- LNA for LTE reception in smart phones, feature phones, tablet PCs and RF front-end modules.

1.4 Quick reference data

Table 1. Quick reference data

f = 882 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)} \geq 0.8$ V; T_{amb} = 25 °C; input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see Figure 4 unless otherwise specified.

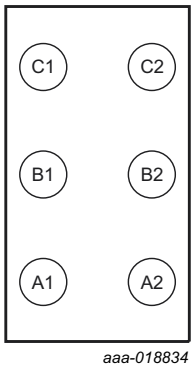
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			1.5	-	3.1	V
I_{CC}	supply current	in gain mode		-	4.4	-	mA
		in bypass mode; 0.1 V ≤ $V_{I(CTRL)}$ ≤ 0.3 V		-	-	1	μA
G_p	power gain	in gain mode	[1]	-	17.3	-	dB
		in bypass mode	[1]	-	–1.8	-	dB
NF	noise figure		[1][2]	-	0.8	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression		[1]	-	–5.0	-	dBm
$IP3_i$	input third-order intercept point		[1]	-	1.0	-	dBm

[1] E_UTRA operating band 5 (869 MHz to 894 MHz).

[2] PCB losses are subtracted.

2. Pinning information

2.1 Pinning



Bump side view

Fig 1. Bump mapping

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2.2 Pin description

Table 2. Ball description

Symbol	Pad	Description
GND	A1	ground
V_{CC}	B1	supply voltage
RF_OUT	C1	RF out
CTRL	A2	gain control, switch between gain and bypass mode
RF_IN	B2	RF in
GND_RF	C2	ground RF

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BGS8L4UK	WLCSP6	wafer level chip-scale package; 6 bumps; 0.69 × 0.44 × 0.29 mm	SOT1445-1

4. Marking

Table 4. Marking codes

Type number	Marking code
BGS8L4UK	single character, indicating assembly month.[1]

[1] Month code see Table 5.

Table 5. Calender marking month code

Asterisk (*) is replaced by character in table, see Figure 2.

Year [1]	Month											
	J	F	M	A	M	J	J	A	S	O	N	D
2015	A	B	C	D	E	F	G	H	I	J	K	L
2016	M	N	O	P	Q	R	S	T	U	V	W	X
2017	Y	Z	b	d	f	h	3	4	5	6	7	8

[1] Rotates every 3 years.

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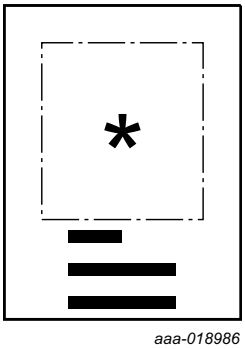

Pin A1 location: the marking stripes below character indicate the side where pin A1 is located.

Fig 2. Marking code description

5. Block diagram

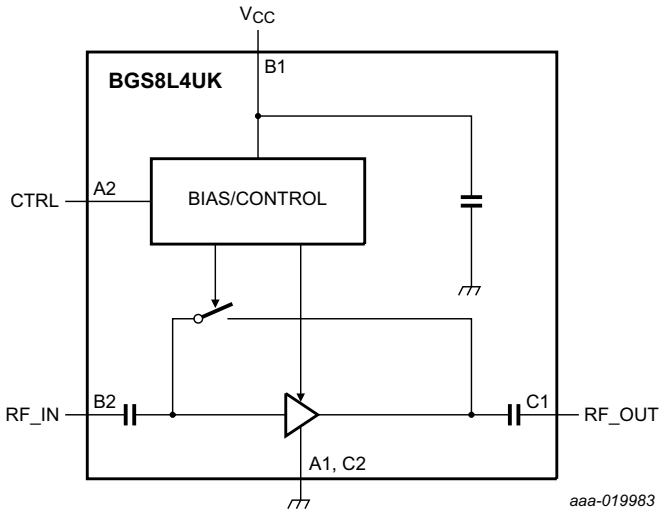

Fig 3. Block diagram

6. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		[1]	–0.5	+5.0	V
$V_{I(CTRL)}$	input voltage on pin CTRL	$V_{I(CTRL)} < V_{CC} + 0.6$ V	[1][2]	–0.5	+5.0	V
$V_{I(RF_IN)}$	input voltage on pin RF_IN	DC, $V_{I(RF_IN)} < V_{CC} + 0.6$ V	[1][2][3]	–0.5	+5.0	V
$V_{I(RF_OUT)}$	input voltage on pin RF_OUT	DC, $V_{I(RF_OUT)} < V_{CC} + 0.6$ V	[1][2][3]	–0.5	+5.0	V
P_i	input power		[1]	-	10	dBm

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Table 6. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).
Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{sp} \leq 130$ °C	-	55	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) According to ANSI/ESDA/JEDEC standard JS-001	-	±2	kV
		Charged Device Model (CDM) According to JEDEC standard JESD22-C101C	-	±1	kV

[1] Stressed with pulses of 200 ms in duration.

[2] Warning: due to internal ESD diode protection, the applied DC voltage shall not exceed V_{CC} + 0.6 V and shall not exceed 5.0 V in order to avoid excess current.

[3] The RF input and output are AC coupled through internal DC blocking capacitors.

7. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		–40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	OFF state	-	-	0.25	V
		ON state	0.8	-	-	V

8. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

9. Characteristics

Table 9. Characteristics

720 MHz ≤ f ≤ 960 MHz; V_{CC} = 1.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)} \geq 0.8$ V	-	4.2	-	mA
G_p	power gain	f = 740 MHz [1]	-	16	-	dB
		f = 882 MHz [2]	-	17	-	dB
		f = 943 MHz [3]	-	17	-	dB

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Table 9. Characteristics *...continued*

720 MHz ≤ f ≤ 960 MHz; V_{CC} = 1.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RL_{in}	input return loss	f = 740 MHz	[1]	-	7	-	dB
		f = 882 MHz	[2]	-	10	-	dB
		f = 943 MHz	[3]	-	11	-	dB
RL_{out}	output return loss	f = 740 MHz	[1]	-	8	-	dB
		f = 882 MHz	[2]	-	15	-	dB
		f = 943 MHz	[3]	-	15	-	dB
ISL	isolation	f = 740 MHz	[1]	-	25	-	dB
		f = 882 MHz	[2]	-	25	-	dB
		f = 943 MHz	[3]	-	25	-	dB
NF	noise figure	f = 740 MHz	[1][4]	-	0.8	-	dB
		f = 882 MHz	[2][4]	-	0.8	-	dB
		f = 943 MHz	[3][4]	-	0.85	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 740 MHz	[1]	-	−8.5	-	dBm
		f = 882 MHz	[2]	-	−9.5	-	dBm
		f = 943 MHz	[3]	-	−9.5	-	dBm
$IP3_i$	input third-order intercept point	f = 740 MHz	[1]	-	−0.5	-	dBm
		f = 882 MHz	[2]	-	0.5	-	dBm
		f = 943 MHz	[3]	-	0.5	-	dBm
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON, to 90 % of the gain		-	-	4	μs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF, to 10 % of the gain		-	-	1	μs
Bypass mode							
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V		-	-	1	μA
G_p	power gain	f = 740 MHz	[1]	-	−1.7	-	dB
		f = 882 MHz	[2]	-	−1.9	-	dB
		f = 943 MHz	[3]	-	−2.1	-	dB
RL_{in}	input return loss	f = 740 MHz	[1]	-	15.3	-	dB
		f = 882 MHz	[2]	-	11.8	-	dB
		f = 943 MHz	[3]	-	10.8	-	dB
RL_{out}	output return loss	f = 740 MHz	[1]	-	13.5	-	dB
		f = 882 MHz	[2]	-	12	-	dB
		f = 943 MHz	[3]	-	11.5	-	dB

[1] E_UTRA operating band 17 (734 MHz to 746 MHz).

[2] E_UTRA operating band 5 (869 MHz to 894 MHz).

[3] E_UTRA operating band 8 (925 MHz to 960 MHz).

[4] PCB losses are subtracted

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Table 10. Characteristics

720 MHz ≤ f ≤ 960 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Gain mode							
I_{CC}	supply current	$V_{I(CTRL)}$ ≥ 0.8 V		-	4.4	-	mA
G_p	power gain	f = 740 MHz	[1]	-	16.1	-	dB
		f = 882 MHz	[2]	-	17.3	-	dB
		f = 943 MHz	[3]	-	17.3	-	dB
RL_{in}	input return loss	f = 740 MHz	[1]	-	7.5	-	dB
		f = 882 MHz	[2]	-	10.5	-	dB
		f = 943 MHz	[3]	-	11.0	-	dB
RL_{out}	output return loss	f = 740 MHz	[1]	-	8	-	dB
		f = 882 MHz	[2]	-	15	-	dB
		f = 943 MHz	[3]	-	15	-	dB
ISL	isolation	f = 740 MHz	[1]	-	25	-	dB
		f = 882 MHz	[2]	-	25	-	dB
		f = 943 MHz	[3]	-	25	-	dB
NF	noise figure	f = 740 MHz	[1][4]	-	0.80	-	dB
		f = 882 MHz	[2][4]	-	0.80	-	dB
		f = 943 MHz	[3][4]	-	0.80	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 740 MHz	[1]	-	−4.5	-	dBm
		f = 882 MHz	[2]	-	−5.0	-	dBm
		f = 943 MHz	[3]	-	−5.0	-	dBm
$IP3_i$	input third-order intercept point	f = 740 MHz	[1]	-	−1.0	-	dBm
		f = 882 MHz	[2]	-	1.0	-	dBm
		f = 943 MHz	[3]	-	0.5	-	dBm
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON, to 90 % of the gain		-	-	4	μs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF, to 10 % of the gain		-	-	1	μs
Bypass mode							
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V		-	-	1	μA
G_p	power gain	f = 740 MHz	[1]	-	−1.5	-	dB
		f = 882 MHz	[2]	-	−1.8	-	dB
		f = 943 MHz	[3]	-	−1.9	-	dB
RL_{in}	input return loss	f = 740 MHz	[1]	-	15.0	-	dB
		f = 882 MHz	[2]	-	12.0	-	dB
		f = 943 MHz	[3]	-	11.0	-	dB

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Table 10. Characteristics *...continued*

720 MHz ≤ f ≤ 960 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see Figure 4 unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RL_{out}	output return loss	f = 740 MHz	[1]	-	12.5	-	dB
		f = 882 MHz	[2]	-	11	-	dB
		f = 943 MHz	[3]	-	10.0	-	dB

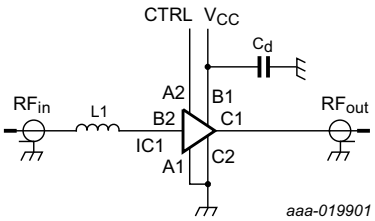
[1] E_UTRA operating band 17 (734 MHz to 746 MHz).

[2] E_UTRA operating band 5 (869 MHz to 894 MHz).

[3] E_UTRA operating band 8 (925 MHz to 960 MHz).

[4] PCB losses are subtracted

10. Application information



For a list of components see Table 11

Fig 4. Schematics LTE LNA evaluation board

Table 11. List of components

Component	Description	Value	Remark
Cd	decoupling capacitor	1 μF	to suppress power supply noise
IC1	BGS8L4UK	-	NXP Semiconductors N.V.
L1	high-quality matching inductor	8.2 nH	Murata LQW15A

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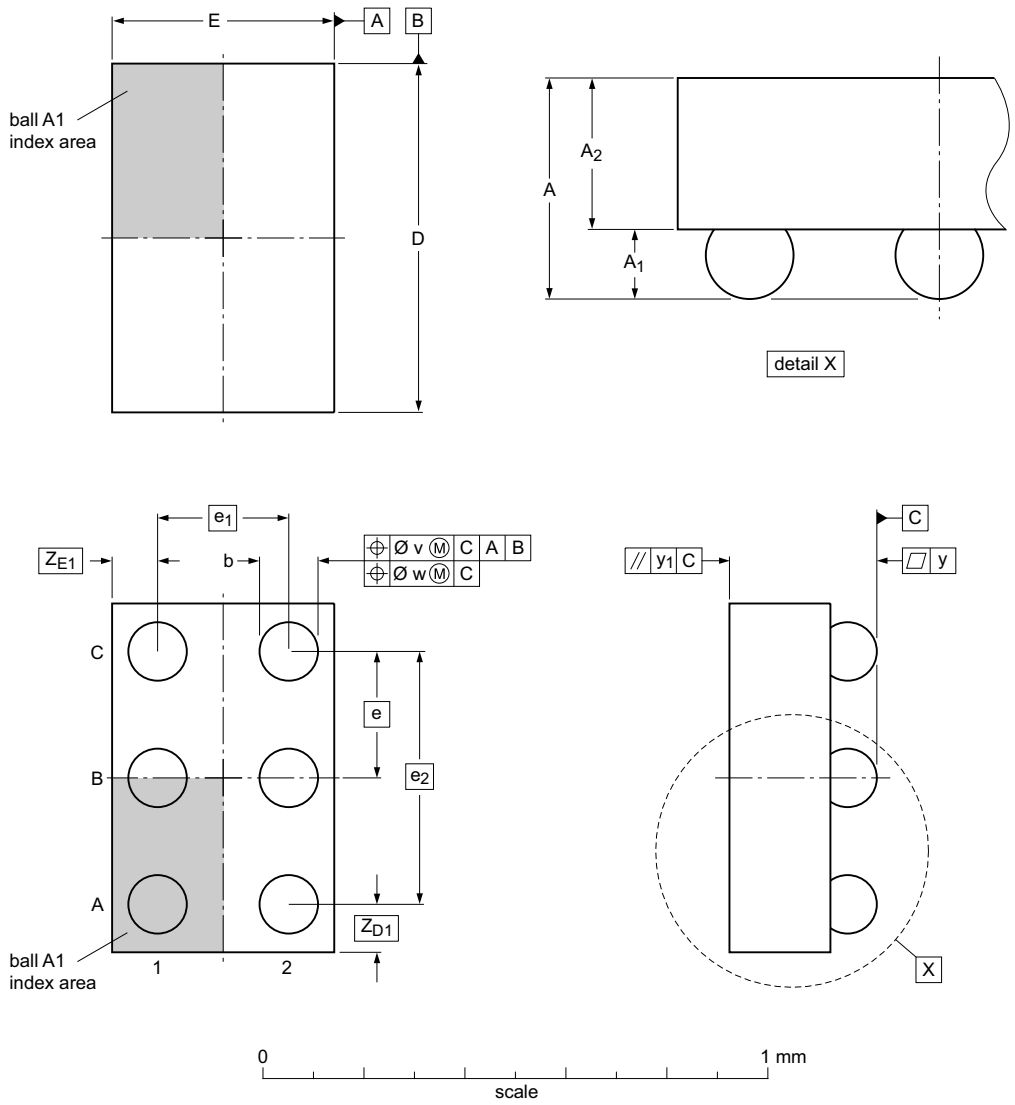
11. Package outline

WLCSP6: wafer level chip-scale package; 6 bumps; 0.69 x 0.44 x 0.29 mm **SOT1445-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1	Z_{D1}	Z_{E1}
mm	max	0.31	0.105	0.215	0.131	0.705	0.455								0.105	0.10
	nom	0.29	0.090	0.200	0.116	0.690	0.440	0.25	0.26	0.50	0.15	0.05	0.03	0.05	0.095	0.09
	min	0.27	0.075	0.185	0.101	0.675	0.425								0.085	0.08

sot1445-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1445-1						~~15-04-28~~ 15-05-11

Fig 5. Package outline SOT1445-1 (WLCSP6)

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12. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

13. Mounting

This WLCSP is only to be used in an overmolded module (using MUF)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MUF	Molded UnderFill
PCB	Printed-Circuit Board
SiGe:C	Silicon Germanium Carbon

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGS8L4UK v.1	20151201	Product data sheet	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 2
1.4 Quick reference data 2
2 Pinning information 2
2.1 Pinning 2
2.2 Pin description 3
3 Ordering information 3
4 Marking 3
5 Block diagram 4
6 Limiting values 4
7 Recommended operating conditions 5
8 Thermal characteristics 5
9 Characteristics 5
10 Application information 8
11 Package outline 9
12 Handling information 10
13 Mounting 10
14 Abbreviations 10
15 Revision history 10
16 Legal information 11
16.1 Data sheet status 11
16.2 Definitions 11
16.3 Disclaimers 11
16.4 Trademarks 12
17 Contact information 12
18 Contents 13

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